S&H Form: PTO/SB/05 (12/97)

JC605 U.S. PTO 08/10/98

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	1317.1043/MDS
First Named Inventor or Application Identifier: Hoon-Soon CHOI	
Express Mail Label No.	

JC540 U.S. PTO 09/131693 08/10/98

APPLICATION ELEMENTS *See MPEP chapter 600 concerning utility patent application contents.*	*ADDRESS TO:* **Assistant Commissioner for Patents Box Patent Application Washington, DC 20231**

1. [X] Fee Transmittal Form
2. [X] Specification, Claims & Abstract ..... [Total Pages: 13]
3. [X] Drawing(s) *(35 USC 113)* ..... [Total Sheets: 5]
4. [X] Oath or Declaration ..... [Total Pages: 1]
   a. [X] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional with Box 17 completed)*
      i. [ ] DELETION OF INVENTOR(S)
      Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. [ ] Incorporation by Reference (usable if Box 4b is checked)
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. [ ] Microfiche Computer Program *(Appendix)*
7. [ ] Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Copy
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   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [X] Assignment Papers (cover sheet & document(s))
9. [ ] 37 CFR 3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12. [ ] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
14. [ ] Small Entity Statement(s) [ ] Statement filed in prior application, status still proper and desired.
15. [X] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. [ ] Other:

17. If a CONTINUING APPLICATION, *check appropriate box and supply the requisite information:*

[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No: ___/_____

18. CORRESPONDENCE ADDRESS

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S&H Form (12/97)

NEW APPLICATION FEE TRANSMITTAL		Attorney Docket No.	1317.1043/MDS
		Application Number	unassigned
		Filing Date	August 10, 1998
AMOUNT ENCLOSED	$ 912.00	First Named Inventor	Hoon-Soon CHOI

FEE CALCULATION (fees effective 10/01/97)

CLAIMS	(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) CALCULATIONS
	TOTAL CLAIMS	19 - 20 =	0	X $ 22.00 =	$ 0.00
	INDEPENDENT CLAIMS	4 - 3 =	1	X $ 82.00 =	82.00
	MULTIPLE DEPENDENT CLAIMS (any number; if applicable)			+ $270.00 =	
			BASIC FILING FEE		+ 790.00
			Total of above Calculations =		$ 872.00
	Surcharge for late filing fee, Statement or Power of Attorney ($130.00)				+
	Reduction by 50% for filing by small entity (37 CFR 1.9, 1.27 & 1.28).				-
			TOTAL FILING FEE =		$ 872.00
	Surcharge for filing non-English language application ($130.00; 37 CFR 1.52(d))				+
	Recordation of Assignment ($40.00; 37 CFR 1.21(h)(1))				+ 40.00
			TOTAL FEES DUE =		$ 912.00

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[X] Check enclosed as payment.

[ ] Charge "TOTAL FEES DUE" to the Deposit Account No., below.

[ ] No payment is enclosed and no charges to the Deposit Account are authorized at this time.

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Deposit Account No.	19-3935
Deposit Account Name	STAAS & HALSEY

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SUBMITTED BY: STAAS & HALSEY

Typed Name	Michael D. Stein	Reg. No.	37,240
Signature		Date	8/10/98

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09453858

TITLE OF THE INVENTION

COMBINED DVD/CD DATA PROCESSOR

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a DVD/CD player, and more particularly, to a combined DVD/CD data processor for use in the DVD/CD player.

2. Description of the Related Art

A DVD (Digital Video Disk) player includes optical and servo systems of which functions and structures are similar to those used in a CD (Compact Disk) player. Therefore, in order to offer convenience to a user, there has been a demand for a DVD player compatible with the CD player.

FIG. 1 illustrates a schematic block diagram of a combined DVD and CD player according to the state of the art. As illustrated, a spindle motor 12 rotates a disk 10 which is a DVD or a CD. An optical pickup 14 reads an RF (Radio Frequency) signal from the disk 10, and an RF amplifier 16 converts the RF signal read by the pickup 14 into a pulse stream, to generate an EFM (Eight to Fourteen Modulated) signal. A microprocessor 20 sets the DVD/CD player to a DVD mode or a CD mode, according to lead-in information received from the RF amplifier 16. A data processor 18 processes the EFM signal according to the set operation mode.

FIG. 2 illustrates the data processor 18 according to the prior art. In operation, the EFM signal is applied in common to a phase locked loop (hereinafter, referred to as PLL)24, a DVD data processor 26, and a CD data processor 38. The PLL 24 generates a PLL clock in synchronism with the EFM signal. The PLL clock is used for reproducing data recorded on the disk 10.

If the microprocessor 20 sets the DVD/CD player to the DVD or the CD mode according to the lead-in information, one of the DVD data processor 26 and the CD data processor 38 is selectively driven.

The DVD data processor 26 includes a frame/ID (Identification) synchronization detector 28, an EFM+ (Eight to Fourteen Modulation Plus) demodulator 30, an RS (Reed-Solomon) decoder 34, an external memory 32, and a descrambler 36. The frame/ID synchronization detector 28 detects a synchronization pattern from the EFM signal to generate a symbol clock to the EFM+ demodulator 30. The EFM+ demodulator 30 EFM+ demodulates the EFM signal according to the symbol clock, and stores the demodulated data into the external memory 32. If the demodulated data stored in the external memory 32 becomes as large as an ECC (Error Checking and Correction) block size, the RS decoder 34 reads the demodulated data with the ECC block size and RS-decodes it to correct errors of the data. The error corrected data is stored back into the external memory 32. The descrambler 36 reads the error corrected data stored in the external memory 32 to descramble the read data and provide the same to an external ATAPI (AT Attachment Packet Interface). Here, in case the DVD/CD player is set to the DVD mode, the descrambled (output) data is applied to an AV (Audio-Visual) decoder.

The CD data processor 38 includes a frame/ID synchronization detector 40, an EFM demodulator 42, an internal memory 44, a deinterleaver 46, a CIRC (Cross Interleave Reed Solomon Code) decoder 48, and an audio processor 50. The frame/ID synchronization detector 40 detects the synchronization pattern from the EFM signal to generate a symbol clock to the EFM demodulator 42. The EFM demodulator 42 EMF-demodulates the EFM signal according to the symbol clock. The demodulated data is deinterleaved by the deinterleaver 46 and stored into the internal memory 44. If the demodulated and deinterleaved data stored in the internal memory 44 reaches a predetermined size, the CIRC decoder 48 reads the demodulated data from the internal memory 44 and CIRC-decodes it to correct errors of the data. The audio processor 50 processes the error corrected data.

As described above, the conventional DVD/CD player includes the DVD data processor 26 and the CD data processor 38 separately, and drives one of them according to the set operation mode, which results into an increase of the complexity of the device, as well as the manufacturing cost.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a combined DVD and CD data processor for use in a DVD/CD player.

Additional objects and advantages of the invention will be set forth in part in the description which follows and, in part, will be obvious from the description, or may be learned by practice of the invention.

To achieve the above and other objects and advantages of the present invention, there is provided a combined DVD/CD data processor used in a DVD/CD player. The DVD/CD data processor includes a PLL to receive a pulse stream input to generate a PLL clock; a frame/ID synchronization detector to latch the pulse stream according to the PLL clock, to generate a symbol clock; a demodulator to EFM+ demodulate the pulse stream according to the symbol clock in a DVD mode, and to EFM demodulate the pulse stream according to the symbol clock in a CD mode; a memory to store the demodulated data; an ECC demodulator to error-correct the demodulated data stored in the memory according to a predetermined code length and error correction range, the predetermined code length and error correction range having different values in the DVD and CD modes; a descrambler to descramble the error corrected data stored in the memory, in the DVD mode; and a CD audio processor to process the error corrected data stored in the memory, in the CD mode.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects and advantages of the present invention will become more apparent by describing in detail a preferred embodiment thereof, with reference to the attached drawings in which:

FIG. 1 is a schematic block diagram of a general DVD/CD player;

FIG. 2 is a detailed block diagram of a data processor of FIG. 1 according to the prior art;

FIG. 3 is a detailed block diagram of a data processor according to an embodiment of the present invention;

FIGS. 4 and 5 are diagrams illustrating memory maps of an external memory of FIG. 3 according to the embodiment of the present invention; and

FIG. 6 is a detailed block diagram of an ECC decoder shown in FIG. 3 according to the embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

A preferred embodiment of the present invention will be described in detail, and it should be noted that like reference numerals denote the same components, and a detailed description of known function and structure of the present invention will be avoided if it is deemed to obscure the subject matter of the present invention.

A combined DVD/CD data processor according to the present invention is applicable to the DVD/CD player shown in FIG. 1, and the microprocessor 20 provides the DVD/CD data processor (the data processor 18 in FIG. 1) with mode setting information for setting the DVD or CD mode.

Referring to FIG. 3, the DVD/CD data processor according to an embodiment of the present invention includes a PLL 52, a frame/ID synchronization detector 54, an EFM/EFM+ demodulator 56, an external memory 58 including a DRAM (dynamic random access memory), a descrambler 60, an ECC decoder 62, and a CD audio processor 64.

The PLL 52 receives the EFM signal from the RF amplifier 16 to generate a PLL clock for restoring data, in synchronism with the received EFM signal. The frame/ID synchronization detector 54 latches the EFM signal according to the PLL clock, and detects frame synchronization and ID synchronization signals to generate a symbol clock. The EFM/EFM+ demodulator 56 selectively performs EFM or EFM+ demodulation according to the mode setting information generated from the microprocessor 20. That is, if the mode setting information indicates the DVD mode (the microprocessor 20 controls the combined DVD/CD data processor to set the DVD/CD player to a DVD mode or a CD mode according to lead-in information received from the RF amplifier 16 and provides the mode setting information for the EFM/EFM+ demodulator 56, the ECC decoder 62 and the CD audio processor 64), the EFM/EFM+ demodulator 56 EFM+ demodulates the EFM signal according to the symbol clock. On the contrary, if the mode setting information indicates the CD mode, the EFM/EFM+ demodulator 56 EFM demodulates the EFM signal according to the symbol clock. Such demodulated data is stored into the external memory 58.

The external memory 58 has a memory map as shown in FIGs. 4 and 5. In the DVD mode, the external memory 58 has 13 ECC blocks each having 32.25-Kbytes to store 13 ECC blocks, as shown in FIG. 4. The external memory 58 is configured to provide a VBR (Variable Bit Rate) control margin for interfacing VBR coded AV data with an AV decoder (not shown). In the CD mode, a specified part, i.e., 32bytes x 256 frames, of the external memory 58 is used, as shown in FIG. 5.

Referring back to FIG. 3, the ECC decoder 62 reads and corrects the data stored in the external memory 58 according to the mode setting information. The ECC decoder 62 has a construction as shown in FIG. 6.

Referring to FIG. 6, the ECC decoder 62 includes a syndrome generator 66, a modified syndrome calculator 68, an erasure constant generator 70, a modified Euclidean algorithm 72, a Chien search and error correction circuit 74.

In the DVD mode, the syndrome generator 66 sets a code length and a correction range to PI(182,172), PO(208,192) and thereafter, receives data from the external memory 58 to generate a syndrome polynomial S(X). In the CD mode, the syndrome generator 66 sets the code length and correction range to C1(32,28), C2(28,24) and thereafter, receives the data from the external memory 58 to generate the syndrome polynomial S(X). The generated syndrome polynomial S(X) is applied to the modified syndrome calculator 68. The erasure constant generator 70 is provided with an erasure flag to generate an erasure constant a^k to the modified syndrome calculator 68. The modified syndrome calculator 68 receives the syndrome polynomial S(X) and the erasure constant a^k to calculate a Forney syndrome polynomial T(X) and an erasure locator polynomial E(X). The calculated Forney syndrome polynomial T(X) and erasure locator polynomial E(X) are applied to the modified Euclidean algorithm 72. The modified Euclidean algorithm 72 processes the Forney syndrome polynomial T(X) and the erasure locator polynomial E(X) based on the modified Euclidean algorithm, to generate an errata locator polynomial W(X) and an errata evaluator polynomial $\Lambda(X)$. The Chien search and error correction circuit 74 receives the errata locator polynomial W(X) and the errata evaluator polynomial $\Lambda(X)$ to correct errors of the corresponding data and store the error corrected data back into the external memory 58.

Since the primitive polynomials for error-correcting the DVD data and the CD data are the same to each other, it is possible to correct the DVD and CD data by controlling only the data received from the syndrome generator 66, with use of the single ECC decoder 62. The primitive polynomial P(X) is represented by:

$$P(X)=x^8+x^4+x^3+x^2+1 \quad \ldots \quad (1)$$

That is, the primitive polynomials for correcting the DVD and CD data are the same to equation (1), and merely, the code lengths and correction ranges of the DVD and CD data to be error-corrected are different from each other. Therefore, by simply controlling the code length and the correction range of the input data according to the set mode, it is possible to correct errors of the DVD and CD data through the use of the single ECC decoder 62.

Referring again to FIG. 3, in the case that the DVD/CD player is set to the DVD mode, the descrambler 60 is enabled to descramble the error corrected data stored in the external memory 58 and provide the descrambled output data to the ATAPI (not shown) or the AV decoder (not shown).

In case the DVD/CD player in set to the CD mode, the CD audio processor 64 is enabled to processes the error corrected data stored in the external memory 58.

As can be appreciated from the foregoing, the DVD/CD data processor according to the present invention includes a single ECC decoder for correcting both the DVD and CD data, and a single external memory. Therefore, the DVD/CD data processor is simple in structure, thereby resulting in a decrease of the manufacturing cost.

While the invention has been shown and described with reference to certain preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims.

CLAIMS

What is claimed is:

1. A combined DVD (Digital Video Disk)/CD (Compact Disk) data processor to process a pulse stream of data from a DVD or a CD, comprising:

a PLL (Phase Locked Loop) to receive the pulse stream, to generate a PLL clock;

a frame/ID (identification) synchronization detector to latch the pulse stream according to said PLL clock, to generate a symbol clock;

a demodulator to EFM+ demodulate the pulse stream according to the symbol clock in a DVD mode, and EFM demodulate the pulse stream according to the symbol clock in a CD mode, to generate demodulated data;

a memory to store the demodulated data from said demodulator;

an ECC (error checking and correction) demodulator to error-correct the demodulated data stored in said memory according to a predetermined code length and error correction range, the predetermined code length and error correction range having different values in the DVD and CD modes, to generate error corrected data;

a descrambler to descramble the error corrected data stored in said memory, in the DVD mode; and

a CD audio processor to process the error corrected data stored in said memory, in the CD mode.

2. The combined DVD/CD data processor as claimed in claim 1, wherein the predetermined code word and correction range in the DVD mode are PI(182,172), PO(208,192), and the predetermined code word and correction range in the CD mode are C1(32,28), C2(28,24).

3. The combined DVD/CD data processor as claimed in claim 2, wherein said ECC demodulator comprises:

a syndrome generator to receive said demodulated data from said memory to generate a syndrome polynomial according to said code length and correction range of PI(182,172), PO(208,192) in the DVD mode, and of C1(32,28), C2(28,24) in the CD mode;

an erasure constant generator to receive an erasure flag to generate an erasure constant;

a modified syndrome calculator to receive the syndrome polynomial and the erasure constant to calculate a modified syndrome and generate a Forney syndrome polynomial and an erasure polynomial;

a modified Euclidean algorithm to process the Forney syndrome polynomial and the erasure polynomial based on a modified Euclidean algorithm, to generate an errata locator polynomial and an errata evaluator polynomial; and

a Chien search and error correction circuit to correct errors of the demodulated data stored in said memory according to said errata locator polynomial and said errata evaluator polynomial.

4. The combined DVD/CD data processor as claimed in claim 1, wherein said memory is an external memory.

5. The combined DVD/CD processor as claimed in claim 1, wherein said memory has a first memory map including a plurality of blocks of the error corrected data each having a first fixed number of bytes in the DVD mode, and a second memory map including a plurality of frames of the error corrected data each having a second fixed number of bytes in the CD mode.

6. The combined DVD/CD processor as claimed in claim 5, wherein:

the plurality of blocks is 13;

the first fixed number of bytes is 32.25Kbytes;

the plurality of frames is 256; and

the second fixed number of bytes is 32bytes.

7. A combined DVD (Digital Video Disk)/CD (Compact Disk) data processor to process first and second pulse streams from a DVD and a CD, respectively, comprising:

a PLL (Phase Locked Loop) to receive the first and second pulse streams, to generate respective first and second PLL clocks;

a frame/ID (identification) synchronization detector to latch the first and second pulse streams according to the respective first and second PLL clocks, to generate respective first and second symbol clocks;

a demodulator to perform a first type of demodulation on the first pulse stream according to the first symbol clock to generate first demodulated data of a DVD mode, and a second type of demodulation on the second pulse stream according to the second symbol clock to generate second demodulated data of a CD mode;

a memory to store the first and second demodulated data; and

an ECC (error checking and correction) demodulator to error correct the first demodulated data stored in said memory in accordance with a first predetermined code length and error correction range and to store the error corrected first demodulated data back in said memory, and to error correct the second demodulated data stored in said memory in accordance with a second predetermined code length and error correction range and to store the error corrected second demodulated data back in said memory.

8. The combined DVD/CD data processor as claimed in claim 7, wherein said memory comprises:

a first memory map to store the error corrected second demodulated data; and

a second memory map different from the first memory map, to store the error corrected second demodulated data.

9. The combined DVD/CD data processor as claimed in claim 8, wherein said first memory map provides a VBR (variable bit rate) control margin to interface the error corrected first demodulated data with an audio/video decoder.

10. The combined DVD/CD data processor as claimed in claim 7, wherein said ECC demodulator comprises:

a syndrome generator to generate syndrome polynomials from the first and second demodulated data stored in said memory in accordance with the corresponding first and second code lengths and corresponding first and second correction ranges;

an erasure constant generator to generate first and second erasure constants from corresponding first and second erasure flags;

a modified syndrome calculator to generate first and second Forney syndrome polynomials and first and second erasure polynomials from the corresponding first and second erasure constants and the corresponding syndrome polynomials;

a modified Euclidean algorithm to process the first and second Forney syndrome polynomials with the corresponding first and second erasure polynomials, to generate corresponding first and second errata locator polynomials and corresponding first and second errata evaluator polynomials; and

a Chien search and error correction unit to correct errors of the first and second demodulated data stored in said memory according to the corresponding first and second errata locator polynomials and the corresponding first and second errata evaluator polynomials.

11. The combined DVD/CD data processor as claimed in claim 7, further comprising:

a descrambler to descramble the error corrected first demodulated data stored in said memory for use with an audio/video decoder; and

an audio processor to audio process the error corrected second demodulated data stored in said memory.

12. A combined DVD (Digital Video Disk)/CD (Compact Disk) data processor to process first and second pulse streams from a DVD and a CD, respectively, comprising:

a demodulator to demodulate the first and second pulse streams in a DVD mode and a CD mode, respectively, to generate first and second demodulated data, respectively;

a memory to store the first and second demodulated data; and

an ECC (error checking and correction) demodulator to error correct the first demodulated data stored in said memory in accordance with a first predetermined code length and error correction range in the DVD mode, and to error correct the second demodulated data stored in said memory in accordance with a second predetermined code length and error correction range in the CD mode.

13. The combined DVD/CD data processor as claimed in claim 12, wherein said memory stores the error corrected first demodulated data output from said ECC demodulator in a first memory map, and the error corrected second demodulated data output from said ECC demodulator in a second memory map different from the first memory map.

14. The combined DVD/CD data processor as claimed in claim 12, further comprising:

a descrambler to descramble the error corrected first demodulated data stored in said memory for use with an audio/video decoder; and

an audio processor to audio process the error corrected second demodulated data stored in said memory.

15. The combined DVD/CD data processor as claimed in claim 12, further comprising:

a PLL (Phase Locked Loop) to receive the first and second pulse streams, to generate respective first and second PLL clocks; and

a frame/ID (identification) synchronization detector to latch the first and second pulse streams according to the respective first and second PLL clocks, to generate respective first and second symbol clocks;

wherein said demodulator performs a first type of demodulation on the first pulse stream according to the first symbol clock to generate the first demodulated data in the DVD mode, and a second type of demodulation on the second pulse stream according to the second symbol clock to generate the second demodulated data in the CD mode.

16. A combined DVD (Digital Video Disk)/CD (Compact Disk) data processor to process first and second pulse streams from a DVD and a CD, respectively, comprising:

a demodulator to demodulate the first and second pulse streams in a DVD mode and a CD mode, respectively, to generate first and second demodulated data, respectively;

a single external memory to store the first and second demodulated data; and

a single ECC (error checking and correction) demodulator to error correct the first and second demodulated data stored in said memory.

17. The combined DVD/CD as claimed in claim 16, wherein said single ECC demodulator error corrects the first and second demodulated data stored in said memory in accordance with corresponding different code lengths and correction ranges.

18. The combined DVD/CD data processor as claimed in claim 16, further comprising:

a descrambler to descramble the error corrected first demodulated data for use with an audio/video decoder; and

an audio processor to audio process the error corrected second demodulated data.

19. The combined DVD/CD data processor as claimed in claim 16, further comprising:

a PLL (Phase Locked Loop) to receive the first and second pulse streams, to generate respective first and second PLL clocks; and

a frame/ID (identification) synchronization detector to latch the first and second pulse streams according to the respective first and second PLL clocks, to generate respective first and second symbol clocks;

wherein said demodulator performs a first type of demodulation on the first pulse stream according to the first symbol clock to generate the first demodulated data in a DVD mode, and a second type of demodulation on the second pulse stream according to the second symbol clock to generate the second demodulated data in a CD mode.

ABSTRACT OF THE DISCLOSURE

A combined DVD/CD (Digital Video Disk/Compact Disk) data processor used in a DVD/CD player. The DVD/CD data processor includes a PLL (Phase Locked Loop) to receive a pulse stream input to generate a PLL clock; a frame/ID synchronization detector to latch the pulse stream according to the PLL clock, to generate a symbol clock; a demodulator to EFM+ demodulate the pulse stream according to the symbol clock in a DVD mode, and EFM demodulate the pulse stream according to the symbol clock in a CD mode; an ECC demodulator to error-correct input data according to a predetermined code length and error correction range, the predetermined code length and error correction range having different values in the DVD and CD modes; a memory to store the demodulated data to provide the ECC demodulator with the demodulated data stored therein; a descrambler to descramble the error corrected data stored in the memory, in the DVD mode; and a CD audio processor to process the error corrected data stored in the memory, in the CD mode.

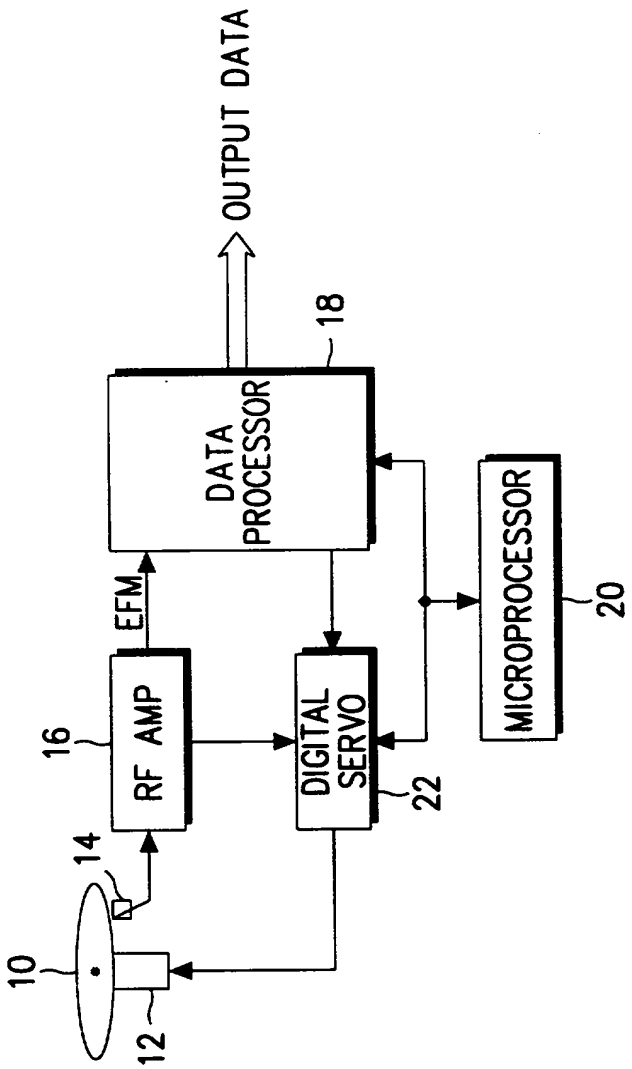

FIG. 1
(PRIOR ART)

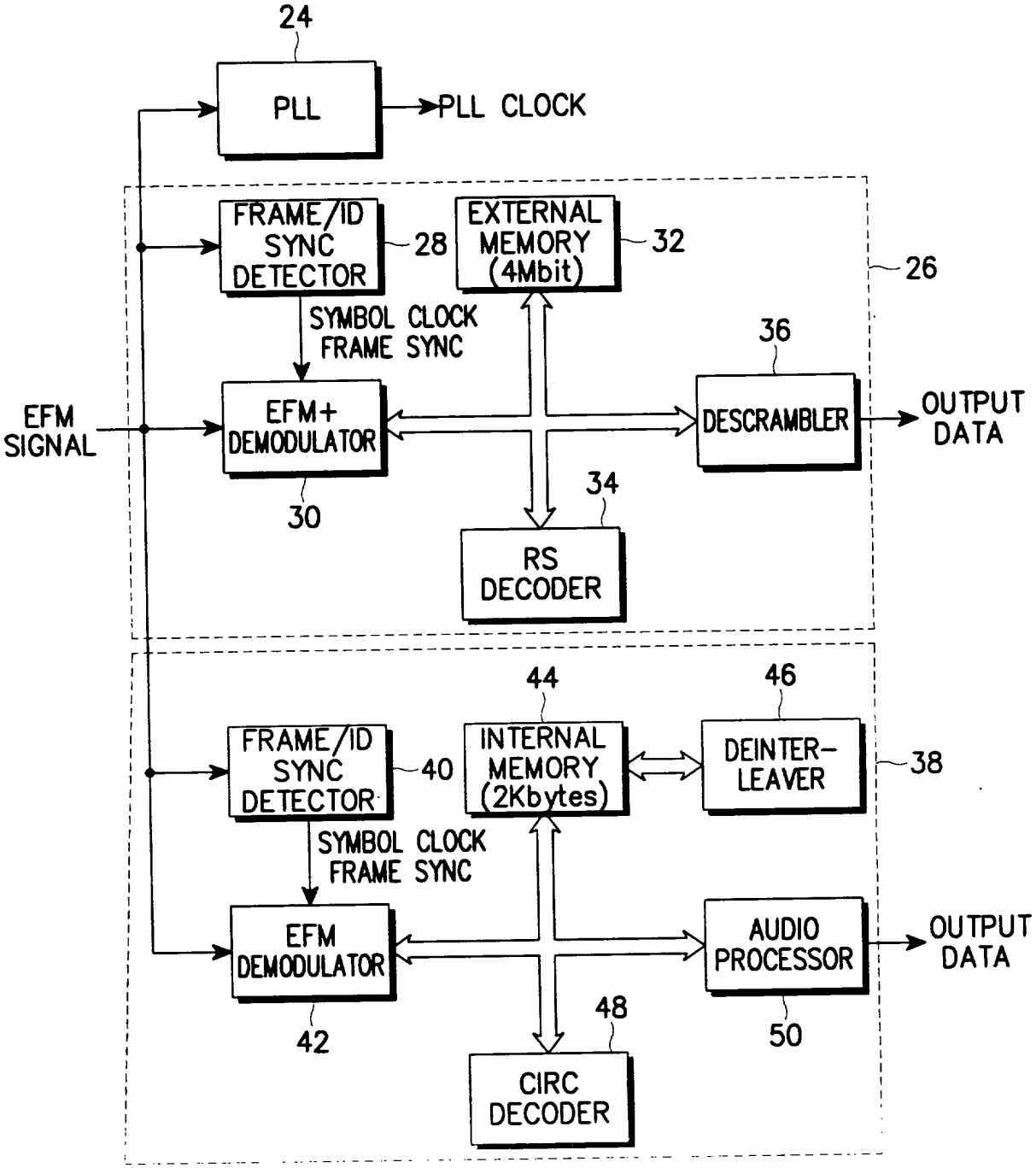

FIG. 2
(PRIOR ART)

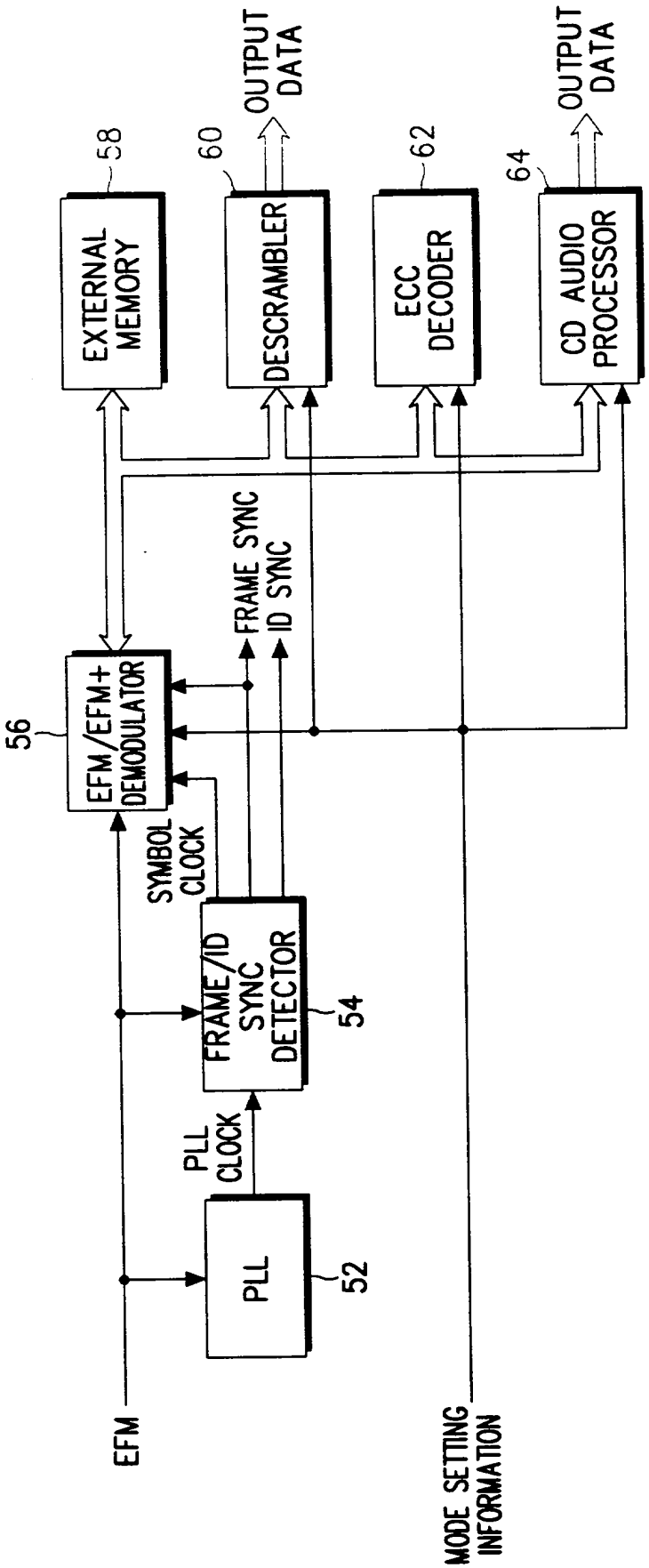
EXTERNAL MEMORY
58
DESCRAMBLER
60
OUTPUT DATA
ECC DECODER
62
CD AUDIO PROCESSOR
64
OUTPUT DATA
EFM/EFM+ DEMODULATOR
56
FRAME SYNC
ID SYNC
SYMBOL CLOCK
FRAME/ID SYNC DETECTOR
54
PLL CLOCK
PLL
52
EFM
MODE SETTING INFORMATION

FIG. 3

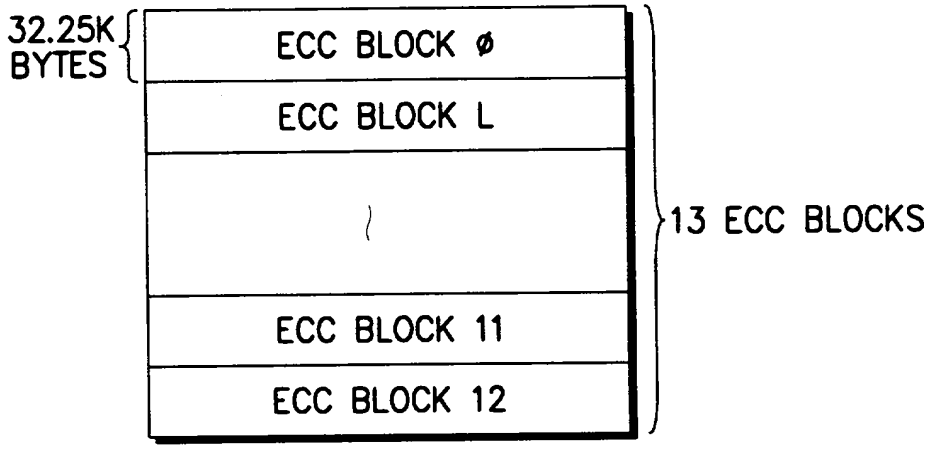
32.25K
BYTES
ECC BLOCK ø
ECC BLOCK L
ECC BLOCK 11
ECC BLOCK 12
13 ECC BLOCKS

FIG. 4

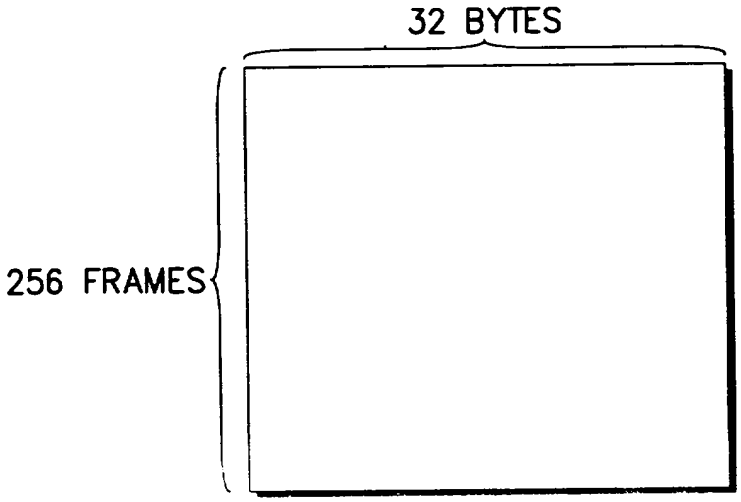
32 BYTES
256 FRAMES

FIG. 5

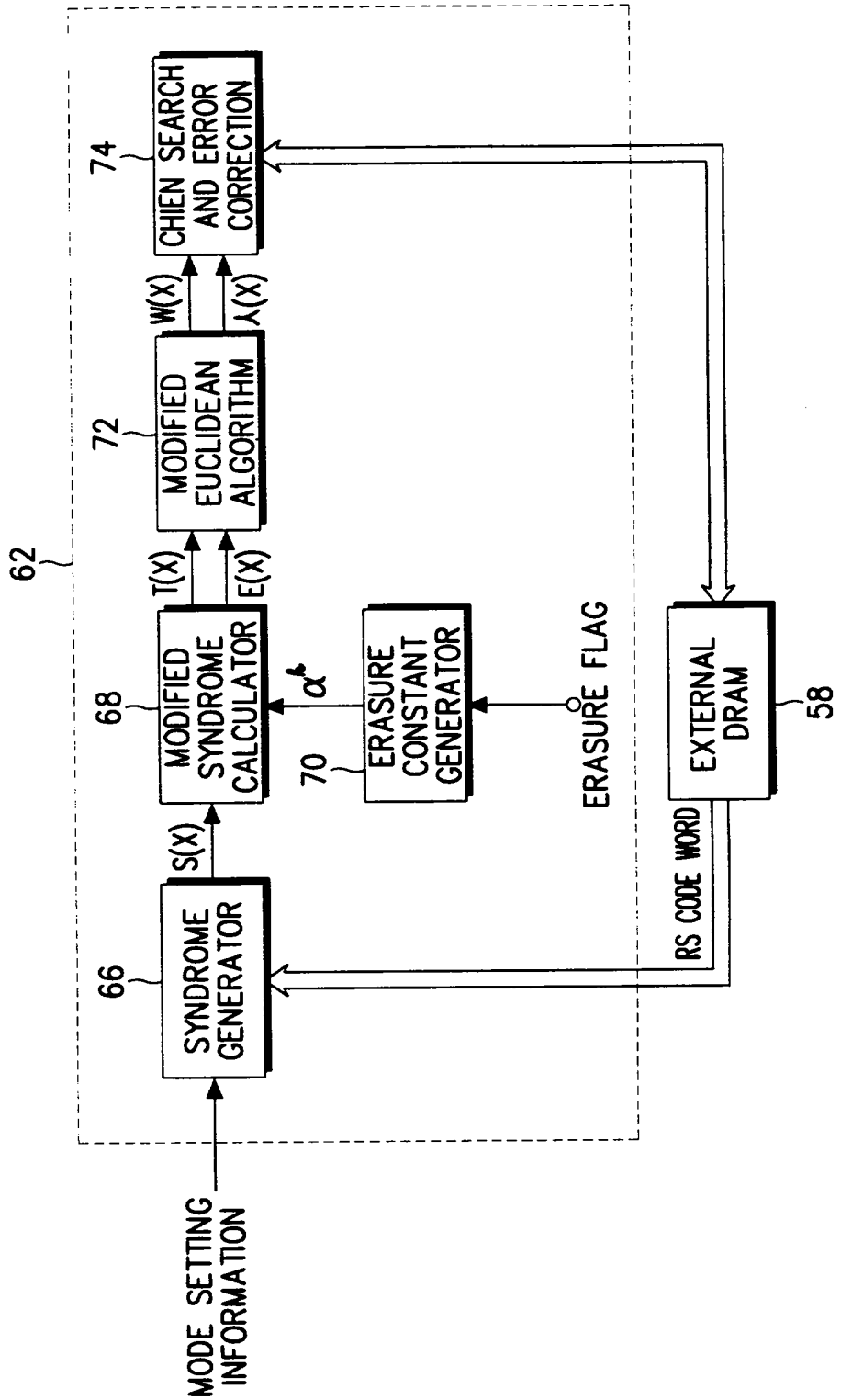
62
MODE SETTING INFORMATION
66
SYNDROME GENERATOR
S(X)
68
MODIFIED SYNDROME CALCULATOR
T(X)
E(X)
70
ERASURE CONSTANT GENERATOR
α^k
ERASURE FLAG
72
MODIFIED EUCLIDEAN ALGORITHM
W(X)
Λ(X)
74
CHIEN SEARCH AND ERROR CORRECTION
58
EXTERNAL DRAM
RS CODE WORD

FIG. 6

S&H 1/97 UNITED STATES Docket No.: _____

COMBINED DECLARATION/POWER OF ATTORNEY FOR UTILITY/DESIGN PATENT APPLICATION

As a below named inventor, I hereby declare that:
My residence, post office address and citizenship are as stated below next to my name.
I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

COMBINED DVD/CD DATA PROCESSOR

the specification of which is attached hereto unless the box is checked:

☐ was filed on _____ as United States Application Number or PCT International Application Number _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.
I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56.
I hereby claim foreign priority benefit(s) under 35 U.S.C. § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application(s) for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s) **Priority Not Claimed**

1997-43697	Korea	30 August, 1997	☐
(Number)	(Country)	Day/Month/Year Filed	
_____	_____	_____	☐
(Number)	(Country)	Day/Month/Year Filed	

☐ I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s), or § 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application(s) in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application.

(Application Serial No.)	(Filing Date)	(Status -- patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status -- patented, pending, abandoned)

I hereby appoint the following attorneys and agent to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. §1001, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor Hoon-Soon CHOI

Inventor's Signature Hoon Soon Choi Date 31 July 1998

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Full name of second joint inventor, if any _____

Second Inventor's Signature _____ Date _____

Residence _____ Citizenship _____

Post Office Address _____

☐ Additional inventors are being named on separately numbered sheets attached hereto.